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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,492	07/16/2003	Majid Movahed Mansoori	TI-35375	9069

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EXAMINER

LINDSAY JR, WALTER LEE

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/620,492

Applicant(s)

MANSOORI ET AL.

Examiner

Walter L. Lindsay, Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) 29-44 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,2,11-13,15-19,21,27 and 28 is/are rejected.
- 7) ☒ Claim(s) 3-10,14,20 and 22-26 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7/16/2003</u> . | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

This Office Action is in response to an Election filed on 9/20/2004.

Currently claims 1-44 are pending. Claims 29-44 have been withdrawn from consideration.

Election/Restrictions

1. Applicant's election without traverse of claims 1-28 in the reply filed on 9/20/2004 is acknowledged.
2. Claims 29-44 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 9/20/2004.

Specification

3. The disclosure is objected to because of the following informalities: In the specification, pages, pages 7 to 8 reference numerals (124) and (126) are used to describe two distinctly different regions in the drawings, (124) is used for overlap capacitance and a dielectric material and (126) is used for overlap capacitance and agate electrode layer, in the prior art section of the application. (See figures 1-8, (prior art)).

Appropriate correction is required.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters (124) and (126) have been use to identify two distinct regions. In Fig. 1 (124) and (126) both represent the overlap capacitance of the gate and the gate dielectric layer. Yet, In Figs. 2 and 3 (124) is a dielectric layer and in Fig. 3 (126) is a gate electrode layer.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

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only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 15 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Dokumaci et al. (U.S. Patent No. 6,686,637 filed 11/21/2002).

Dokumaci shows the method as claimed, in Figs. 1-12 and corresponding text as: forming a layer of poly-SiGe with carbon (102) (col. 4, lines 47-55) [Si/SiGe, embodiment], over a dielectric layer (104) situated on a substrate (106) (Fig. 1) (col. 3, lines 6-19)(col. 4, lines 47-55); forming a layer of poly-Si (116) over the layer of poly-SiGe (Fig. 6) (col. 3, line 62-col. 4, line 10) and patterning the poly-Si, poly-SiGe and dielectric layers to form the gate stack (110/118) (Fig. 10) (col. 4, lines 23-34) (claim 1). Dokumaci teaches that the layer of poly-Si includes carbon (Fig. 11) (col. 4, lines 23-34) [carbon is implanted into 118](claim 2).

Dokumaci shows the method as claimed, in Figs. 1-12 and corresponding text as: forming a layer of dielectric material (104) over a substrate (106) (Fig. 1) (col. 3, lines 6-19); forming a layer of poly-SiGe with carbon (102) over a dielectric layer situated on the substrate (Fig. 1) (col. 3, lines 6-19) (col. 4, lines 47-55); forming a layer of poly-Si (116) over the layer of poly-SiGe (Fig. 6) (col. 3, line 62-col. 4, line 10); patterning the poly-Si (118), poly-SiGe (110) and dielectric layer to form a gate stack (Fig. 10)(col. 4, lines 23-34); and doping exposed portions of the substrate adjacent to the gate stack to form source and drain regions (126) (Fig. 11) (col. 4, lines 11-23) (claim 15). Dokumaci teaches that the layer of poly-Si includes carbon (Fig. 11) (col. 4, lines 23-34) (claim 21) [carbon is implanted into 118].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 11-12 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dokumaci (U.S. Patent No. 6,686,637, filed 11/21/2002) in view of Sagnes (U.S. Patent No. 5,998,289, dated 12/7/1999).

Dokumaci shows the method substantially as claimed and as described in the preceding paragraphs.

Dokumaci lacks anticipation only in not explicitly teaching that: 1) the poly-SiGe layer has a thickness of about 400 to 700 Angstroms (claim 11); 2) the poly-Si layer has a thickness of about 350 to 750 Angstroms (claim 12); 3) the poly-SiGe layer has a thickness of about 400 to 700 Angstroms (claim 27); and 4) the poly-Si layer has a thickness of about 350 to 750 Angstroms (claim 28).

Sagnes teaches a silicon-germanium gate transistor. Sagnes shows the polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ layer having a thickness between 50nm (500 Å) and 200 nm (2000 Å) and thickness of polycrystalline Si is between 50nm (500Å) to 150 nm (1500Å). The SiGe material, has a lower resistance than polycrystalline silicon, offers the possibility of shifting the threshold voltage of a PMOS and can act as a mid-gap material.

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

It would be obvious to one of ordinary skill in the art, at the time the invention was made to modify, the method shown in Dokumaci, where a poly-SiGe layer has a thickness of about 400 to 700 Angstroms and that the poly-Si layer has a thickness of about 350 to 750 Angstroms, as taught by Sagnes, with the motivation that Sagnes teaches that SiGe material has a lower resistance than polycrystalline silicon, offers the possibility of shifting the threshold voltage of a PMOS and can act as a mid-gap material.

11. Claims 13, and 16-19 are rejected under 35 U.S.C. 103(a) as being obvious over Dokumaci et al. (U.S. Patent No. 6,686,637 filed 11/21/2002) in view of Moslehi (U.S. Patent No. 5,397,909 dated 3/14/1995).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(I)(1) and § 706.02(I)(2). Moslehi U.S. Patent No. 5,397,909 patented on 3/14/1995.

Dokumaci shows the method substantially as claimed and as described in the preceding paragraphs.

Dokumaci shows the method substantially as claimed, in Figs. 1-12 and corresponding text and, as previously described including: doping exposed regions of the substrate adjacent the gate stack to form source and drain extension regions (120) before forming the source and drain regions (Fig. 10) (col. 4, lines 11-23) (claim 16). Dokumaci teaches forming sidewall spacers (124) adjacent the gate structure prior to forming the source and drain regions (126), but after forming the source and drain extension regions (Fig. 11) (col. 4, lines 11-23) (claim 17).

Dokumaci lacks anticipation only in not explicitly teaching that: 1) the dielectric layer has a thickness of about 100 Angstroms; 2) the source and drain extension regions are lightly doped relative to the source and drain regions (claim 16); 3) a layer of insulating material is formed over the gate stack and exposed portions of the substrate; and selectively removing portions of the insulating material (claim 18); and 4) the insulating material comprises at least one of silicon nitride and silicon oxide (claim 19).

Moslehi teaches a MOSFET device that employs a double gate, and a lightly doped source drain region. Moslehi forms a dielectric layer (48) on the order of 100 Angstroms (col. 11, lines 25-28) and implants source/drain lightly doped extension region (58) through the dielectric layer before the formation of sidewall spacers (60)(col. 12, lines 41-68). Sidewall spacers (60) are formed by depositing silicon nitride or silicon oxide over the substrate and gate, etching the insulating layer to form the spacers (col. 12, line 67 –col. 13 line 20). Additionally the source/drain region (64) is formed to

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complete the device (col. 13, lines 31-45). The process described by Moslehi lends itself to both p or n-channel devices, it also provides for reduced device punch-through leakage and to reduce degradation of process control due to changes in threshold voltage.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify the method shown in Dokumaci so that the dielectric layer has a thickness of about 100 Angstroms, the source and drain extension regions are lightly doped relative to the source and drain regions, and forming a layer of insulating material over the gatestack and exposed portions of the substrate and selectively removing portions of the insulating material, the insulating material being either silicon nitride or silicon oxide, as taught by Moslehi, with the motivation that Moslehi teaches that both p or n-channel devices can be formed, that a reduction of punch-through leakage is achieved and that degradation of process control due to changes in threshold voltage are reduced.

Allowable Subject Matter

1. Claims 3-10, 14, 20 and 22-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
2. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...forming a polysilicon seed layer over the dielectric layer, as required by claim 3 as it depends from claim 2;

...wherein the seed layer includes carbon, as required by claim 4, as it depends from claim 3;

...wherein the poly-Si, poly-SiGe and seed layers are patterned via an etching process, as required by claim 5, as it depends from claim 4;

...wherein the carbon within the layers changes a passivation material formation and etch rate during the etching process, as required by claim 6, as it depends from claim 5;

...wherein the etching is substantially isotropic due to the change in passivation and etch rate, as required by claim 7, as it depends from claim 6;

...wherein the poly-SiGe layer has a greater etch sensitivity to an etchant utilized to etch the layers in forming the gate structure, as required by claim 8, as it depends from claim 7;

...wherein at least one of the seed layer, poly-SiGe layer and poly-Si layer contains a concentration of carbon between about 0.1 to 1.0 atomic percent, as required by claim 9, as it depends from claim 8;

...wherein the seed layer has a thickness of about 100 Angstroms or less, as required by claim 10, as it depends from claim 3;

...wherein at least one of the dielectric layer, seed layer, poly-SiGe layer and poly-Si layer is formed according to at least one of spin-on techniques, sputtering

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techniques, growth techniques and deposition techniques, as required by claimed 14, as it depends from claim 4;

...forming a polysilicon seed layer over the layer of dielectric material, as required by claim 20 as it depends from claim 15;

...forming a polysilicon seed layer over the dielectric layer, as required by claim 22 as it depends from claim 21;

...wherein the seed layer includes carbon, as required by claim 23, as it depends from claim 22;

...wherein the poly-Si, poly-SiGe and seed layers are patterned via an etching process, and wherein the poly-SiGe layer has a greater etch sensitivity to an etchant utilized to etch the layers, as required by claim 24, as it depends from claim 23

...wherein at least one of the seed layer, poly-SiGe layer and poly-Si layer contains a concentration of carbon between about 0.1 to 1.0 atomic percent, as required by claim 25, as it depends from claim 23; and

...wherein the seed layer has a thickness of about 100 Angstroms or less, as required by claim 26, as it depends from claim 22.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL

Walter L. Lindsay
October 26, 2004

